WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising a memory chip comprising:

a nonvolatile memory cell array;

a write circuit which repeatedly executes a write and a verification on one write unit in the memory cell array to complete a verify write on the write unit; and

a write voltage control circuit which changes a write voltage in each write executed repeatedly by the write circuit, the write voltage control circuit comprising:

a first binary counter which operates after an initial value for a write voltage has been set, to count a first clock signal supplied every time the verification fails and supply output data to the write circuit as data on a write voltage for each verify write;

a first register which stores data for setting the number of writes and verifications on a target write unit;

a second binary counter which is reset using a first timing, counts a second clock signal supplied if a verify write executed on the target write unit fails even though the verify write is repeated a number of times set in the first register, and supplies output data to the first binary counter as an initial value for the write voltage;

a second register which stores the number of write units used for a test for determining an appropriate value for a write start voltage for the memory chip;

an accumulative value storage circuit which is reset using a second timing and stores a value corresponding to an accumulative value for the contents of the second binary counter obtained as a result of the verify write executed on a plurality of write units corresponding to the number of times specified by the second register; and

a nonvolatile storage element which stores the appropriate value for the write start voltage for the memory chip in accordance with stored contents of the accumulative value storage circuit and stored contents of the second register.

2. The nonvolatile semiconductor memory according to claim 1, wherein the first timing corresponds to a point in time when the test is started and a point in time when a number of verify operations performed on the target unit have been completed, the number of verify operations being equal to the number of times set in the first register, and the second timing corresponds to the time when the test is started.

3. The nonvolatile semiconductor memory according to claim 1, wherein the accumulative value storage circuit is a third binary counter which stores the value corresponding to the accumulative value for the

contents of the second binary counter by counting the second clock signal.

4. The nonvolatile semiconductor memory according to claim 1, wherein the nonvolatile storage element stores a value obtained by averaging the stored contents of the accumulative value storage circuit in accordance with the stored contents of the second register, plus an offset voltage.

5. The nonvolatile semiconductor memory according to claim 1, wherein an external input is used to set, in the second register, the number of units on which a test for determining the appropriate value is executed, or the second register counts the number of units on which the test for determining the appropriate value has been executed.

6. The nonvolatile semiconductor memory according to claim 1, wherein during a test, an initial value in the second binary counter is set on the basis of an externally inputted command and is set as an initial value in the first binary counter.

7. The nonvolatile semiconductor memory according to claim 1, wherein in normal operation, the initial value in the second binary counter is set on the basis of the start voltage stored in the nonvolatile storage element and is set as the initial value in the first binary counter.

8. A nonvolatile semiconductor memory comprising

a memory chip comprising:

a nonvolatile memory cell array;

an erase circuit which repeatedly executes an erase and a verification on one erase unit in the memory cell array to complete a verify erase on the erase unit; and

an erase voltage control circuit which changes an erase voltage in each erase executed repeatedly by the erase circuit, the erase voltage control circuit comprising:

a first binary counter which operates after an initial value for an erase voltage has been set, to count a first clock signal supplied every time the verification fails and supply output data to the erase circuit as data on an erase voltage for each verify erase;

a first register which stores data for setting the number of erases and verifications on a target erase unit;

a second binary counter which is reset using a first timing, counts a second clock signal supplied if a verify erase executed on the target erase unit fails even though the verify erase is repeated a number of times set in the first register, and supplies output data to the first binary counter as an initial value for the erase voltage;

a second register which stores the number of erase

units used for a test for determining an appropriate value for an erase start voltage for the memory chip;

an accumulative value storage circuit which is reset using a second timing and stores a value corresponding to an accumulative value for the contents of the second binary counter obtained as a result of the verify erase executed on a plurality of erase units corresponding to the number of times specified by the second register; and

a nonvolatile storage element which stores the appropriate value for the erase start voltage for the memory chip in accordance with stored contents of the accumulative value storage circuit and stored contents of the second register.

9. The nonvolatile semiconductor memory according to claim 8, wherein the first timing corresponds to a point in time when the test is started and a point in time when a number of verify operations performed on the target unit have been completed, the number of verify operations being equal to the number of times set in the first register, and the second timing corresponds to the time when the test is started.

10. The nonvolatile semiconductor memory according to claim 8, wherein the accumulative value storage circuit is a third binary counter which stores the value corresponding to the accumulative value for the contents of the second binary counter by counting the

second clock signal.

11. The nonvolatile semiconductor memory according to claim 8, wherein the nonvolatile storage element stores a value obtained by averaging the stored contents of the accumulative value storage circuit in accordance with the stored contents of the second register, plus an offset voltage.

12. The nonvolatile semiconductor memory according to claim 8, wherein an external input is used to set, in the second register, the number of units on which a test for determining the appropriate value is executed, or the second register counts the number of units on which the test for determining the appropriate value has been executed.

13. The nonvolatile semiconductor memory according to claim 8, wherein during a test, an initial value in the second binary counter is set on the basis of an externally inputted command and is set as an initial value in the first binary counter.

14. The nonvolatile semiconductor memory according to claim 8, wherein in normal operation, the initial value in the second binary counter is set on the basis of the start voltage stored in the nonvolatile storage element and is set as the initial value in the first binary counter.

15. A method used in a nonvolatile semiconductor memory comprising an array of memory cells each having

a control gate and a floating gate and a write voltage generating circuit for which an initial voltage is determined on the basis of data stored in a register, to increase, in writing data to the memory cell, a write voltage provided to the control gate, in increments of a fixed voltage starting with the initial voltage, in each of a plurality of steps into which a write operation is divided, to obtain a write voltage data reflecting characteristics of each semiconductor chip, the method comprising:

setting the number of steps at a predetermined value;

carrying out a self-determination test to start a write operation with a certain initial voltage and output "pass" or "fail" depending on whether or not data has been successfully written in all memory cells in one target write unit;

repeating a process of changing data in the register in a direction in which the initial voltage is increased by a fixed value if a result of the self-determination test is "fail" and causing the self-determination test to be executed with an initial voltage based on the changed data until the initial voltage based on the changed data reaches a predetermined value;

executing on a plurality of write units a process of changing the target write unit after the initial

voltage based on the data changed by the repeating of the process reaches the predetermined value and causing the self-determination test and the process repeating to be executed; and

determining an average value per write unit on the basis of accumulative data obtained by executing writes on the plurality of write units and setting, in the register, write voltage data reflecting the characteristics of each semiconductor chip.

16. The method used in a nonvolatile semiconductor memory according to claim 15, wherein the self-determination test is carried out by an externally inputted command.

17. A method used in a nonvolatile semiconductor memory comprising an array of memory cells each having a control gate and a floating gate formed on a well region and an erase voltage generating circuit for which an initial voltage is determined on the basis of data stored in a register, to increase, in writing data to the memory cell, an erase voltage provided to the well region, in increments of a fixed voltage starting with the initial voltage, in each of a plurality of steps into which an erase operation is divided, to obtain an erase voltage data reflecting characteristics of each semiconductor chip, the method comprising:

setting the number of steps at a predetermined

value;

carrying out a self-determination test to start an erase operation with a certain initial voltage and output "pass" or "fail" depending on whether or not data has been successfully written in all memory cells in one target erase unit;

repeating a process of changing data in the register in a direction in which the initial voltage is increased by a fixed value if a result of the self-determination test is "fail" and causing the self-determination test to be executed with an initial voltage based on the changed data until the initial voltage based on the changed data reaches a predetermined value;

executing on a plurality of erase units a process of changing the target erase unit after the initial voltage based on the data changed by the repeating of the process reaches the predetermined value and causing the self-determination test and the process repeating to be executed; and

determining an average value per erase unit on the basis of accumulative data obtained by executing erases on the plurality of erase units and setting, in the register, erase voltage data reflecting the characteristics of each semiconductor chip.

18. The method used in a nonvolatile semiconductor memory according to claim 17, wherein the

self-determination test is carried out by an externally inputted command.